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DERWENT-ACC-NO: 1998-244038
DERWENT-WEEK: 199822

TITLE: Semiconductor device e.g. transistor with metallic gate electrode - in which first and second metal patterns bearing gate electrode are laminated sequentially over gate insulating film

PATENT-ASSIGNEE:

ASSIGNEE	CODE
SAMSUNG ELECTRONICS CO LTD	SMSU

PRIORITY-DATA:
1995KR-0009451 April 21, 1995

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 08293604 A	November 5, 1996	N/A	008	H01L029/78

APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-NO	APPL-DESCRIPTOR
JP08293604A	January 29, 1996	1996JP-0013256	N/A

INT-CL (IPC): H01L 21/336; H01L 29/78

ABSTRACTED-PUB-NO: JP08293604A
BASIC-ABSTRACT:

The device includes a first electric conduction type semiconductor substrate (60) on whose main surface several field oxide films (62) for element isolation are formed. A gate insulating film (64) is formed on the substrate between field oxide films. A gate electrode which includes a first metal pattern (68a) and a second metal pattern (78) is formed on the gate insulating film. The first metal film pattern is formed from nitrate metal. The second metal film pattern has small specific resistance.

A spacer (76) is formed on both side attachment walls of the gate electrode. The spacer is made from an excellent substance film by which etching selection ratio for etching liquid, of

the oxide film is carried out. A source and drain area (80) in which electrically conductive impurity is doped, is formed on the surface of substrate.

ADVANTAGE - Reduces resistance of wiring. Controls short channel effect of P-channel transistor. Obtains semiconductor device with high integration density.

ABSTRACTED-PUB-NO: JP08293604A
EQUIVALENT-ABSTRACTS:

CHOSEN-DRAWING: Dwg.2/11

DERWENT-CLASS: U11 U12
EPI-CODES: U11-C05D; U11-C05F1; U12-D02A;